Ramon Chips, Haifa, Israel

Technion 1925

2000

Ramon Chips

Ramon Chips is named in memory of Col. Ilan Ramon, Israeli astronaut who died on board the Columbia space shuttle, 1/2/2003

Converting PLD-based SoC into RadSafe™ ASIC

Prof. Ran Ginosar, CEO, Ramon Chips

MAPLD, September 2008

ran@ramon-chips.com

About Ramon Chips

- Private company, incorporated 2004
- Based in Haifa, Israel
- Developed RadSafe™ technology
- Made, qualified and delivered several space grade components
- Focused on ASIC for space
  - Most products FPGA→ASIC conversions
  - Higher reliability and performance at lower cost and power

Outline

- RadSafe™ concepts
- RadSafe™ libraries and cores
- Example FPGA→ASIC conversions

RadSafe™ concepts

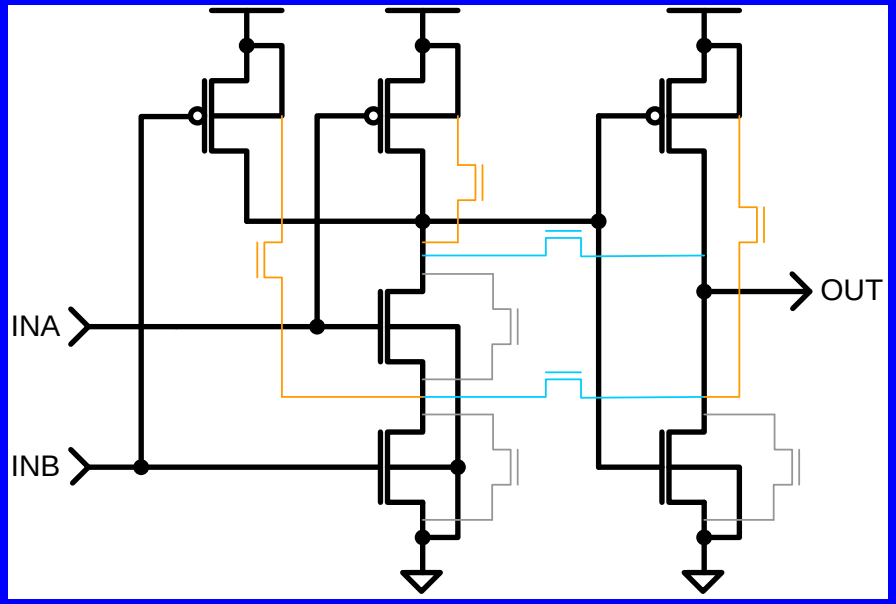
- Rad Hard By Design
- Rad Hard By Similarity
- Commercial CMOS technology
  - Tower Semi 0.18µ CMOS (→ 0.13µ)
- Static CMOS circuits
- Own library (rad hard circuits)
- Own methodology
- Proven Rad Hard, qualifiable

Radiation effects mitigated by RadSafe™

- TID
- SEL
- SEU/SET in flip-flops
- SEU in SRAMs
- SEFI caused by PLL/DLLs

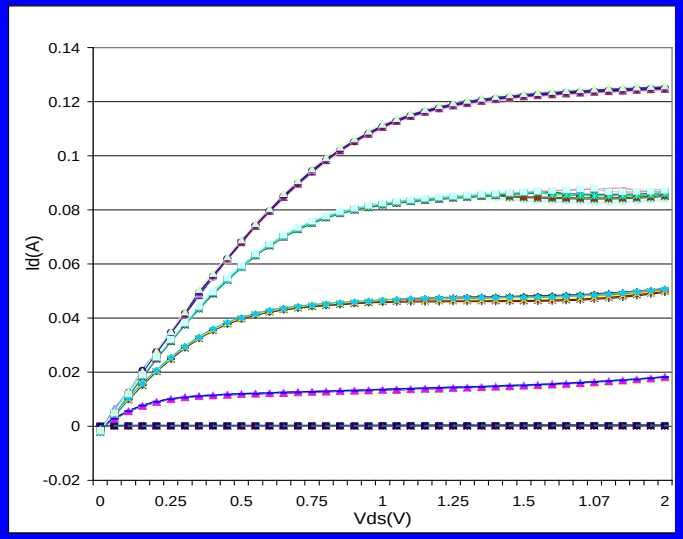
Mitigating TID effects

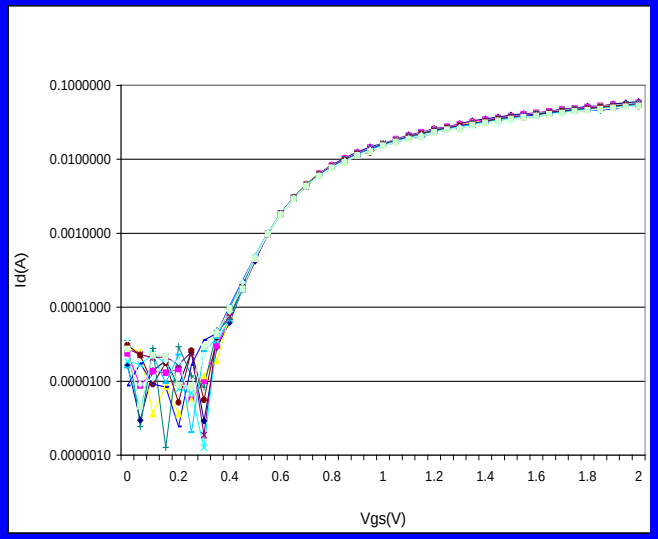
- Advanced CMOS process – *≤0.18µ with STI*
- Fixed layout – *predictable parasitic devices; insensitive to placement*
- Only 30% area penalty
- TID immunity: >300Krad in all tests



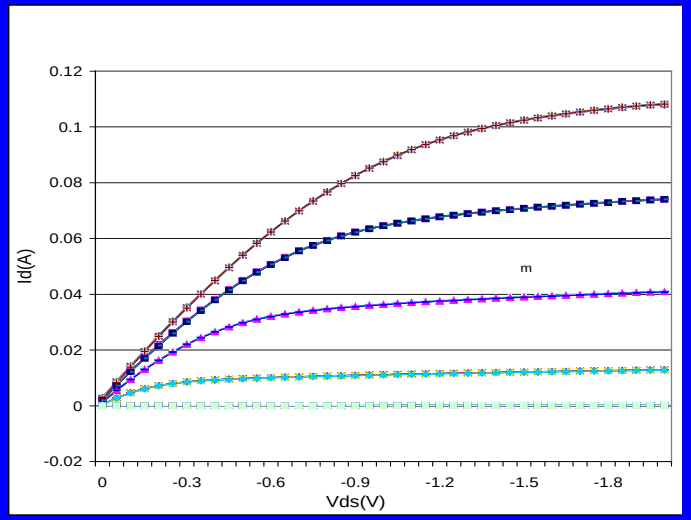
Performance under TID stress

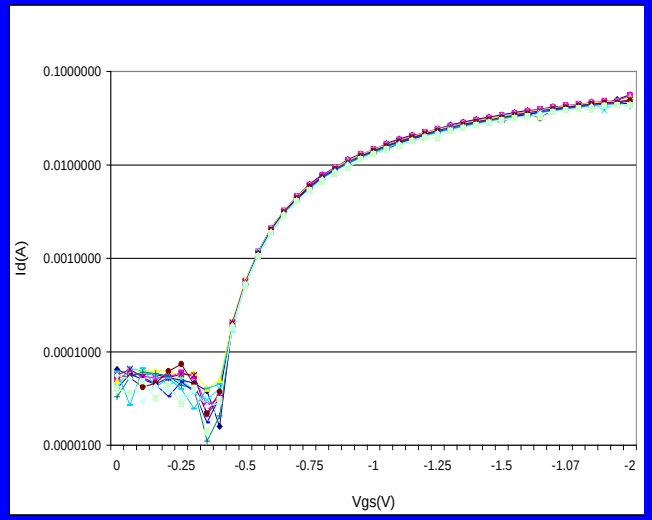
NMOS





PMOS





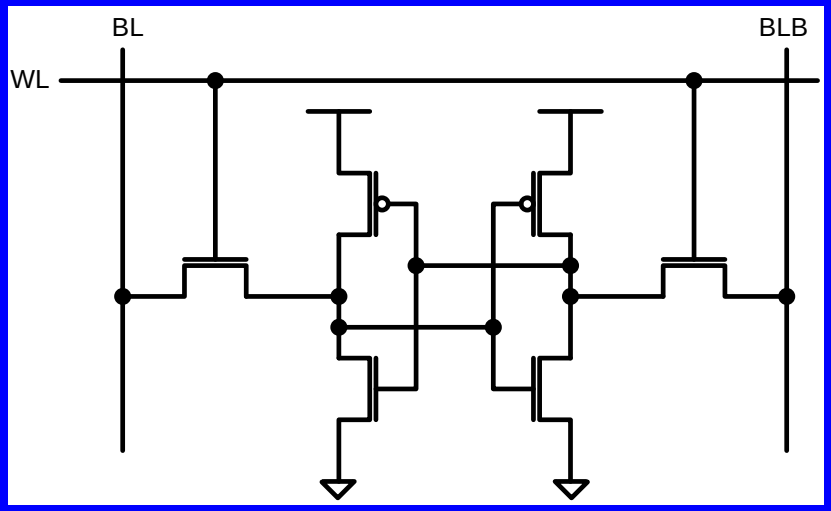
Mitigating SEL

- Fixed PNPN geometry
  - insensitive to placement
- Double/triple guard rings in I/O circuits
- No SEL detected up to 106MeV·cm2/mg

Mitigating SEU in flip-flops

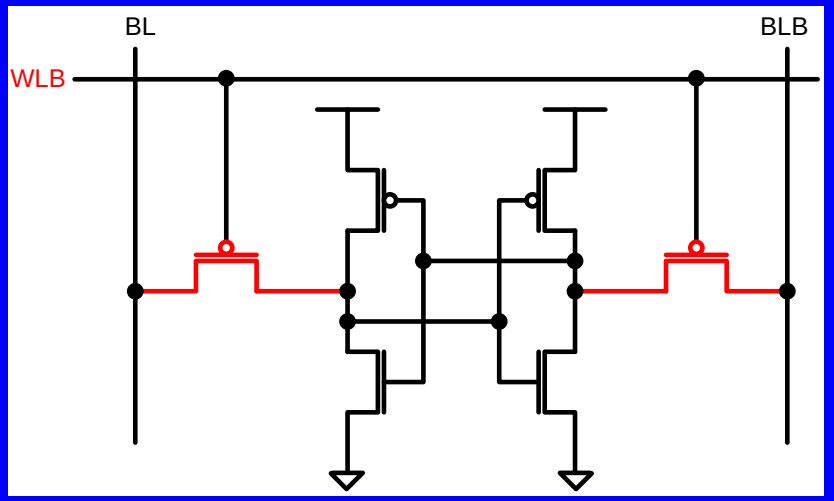
- SEP = Single Error Protected FF
- Continuous self-correcting feedback
  - At each latch (x2)
- SET filter for data
- SET Filter for clock
- SET Filter for async Set/Reset
- All flip-flops tested by SCAN
- Less than 10^{-12} errors/bit/day

RadSafe SRAM cell



Conventional SRAM cell

Many NMOS devices connected to bit-lines

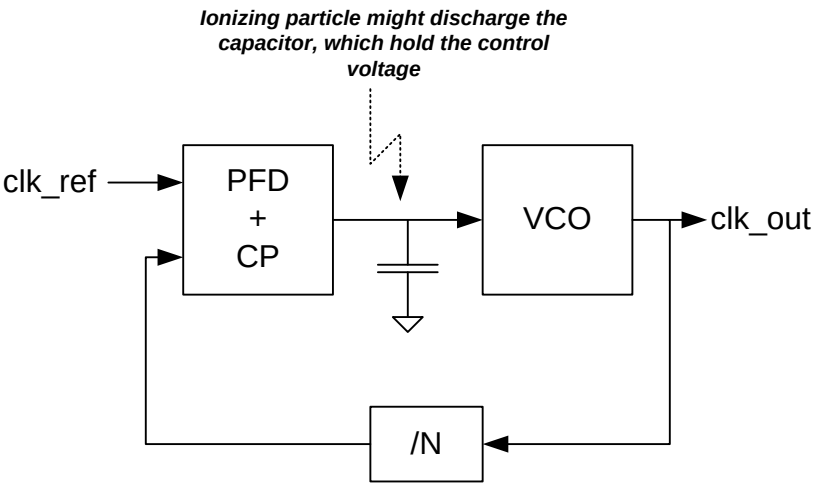


RadSafe™ SRAM cell

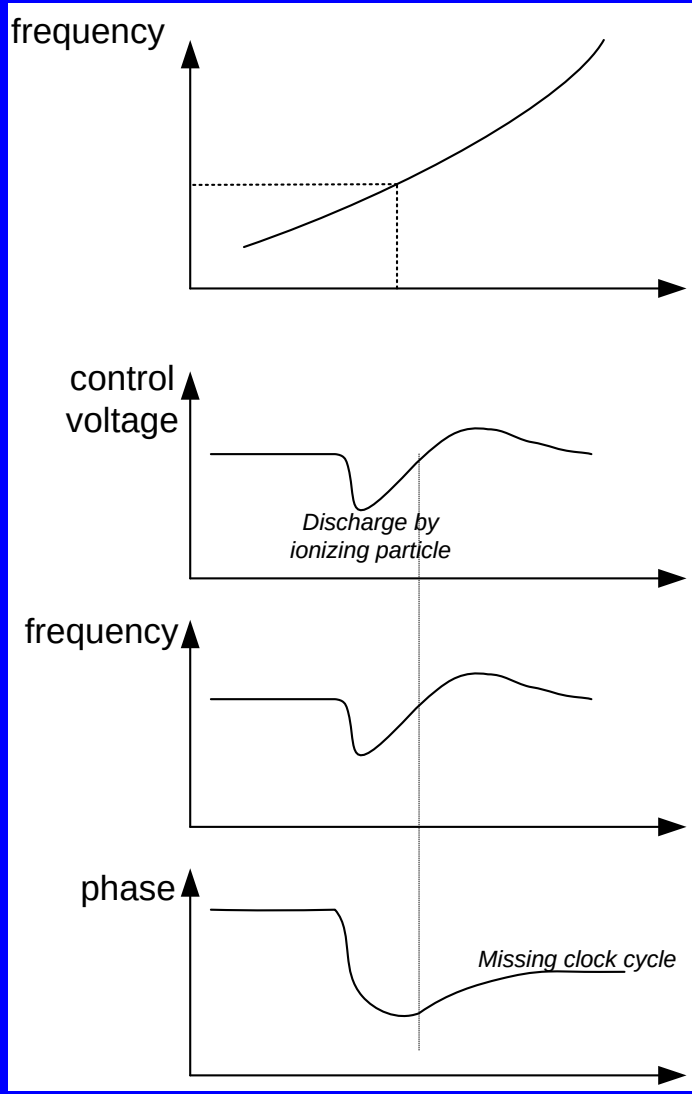
Only PMOS devices connected to bit-lines

- Less than 2×10^{-7} errors/bit/day
- EDAC tested to fix all SEU in SRAM

Analog PLL sensitive to TID, SET

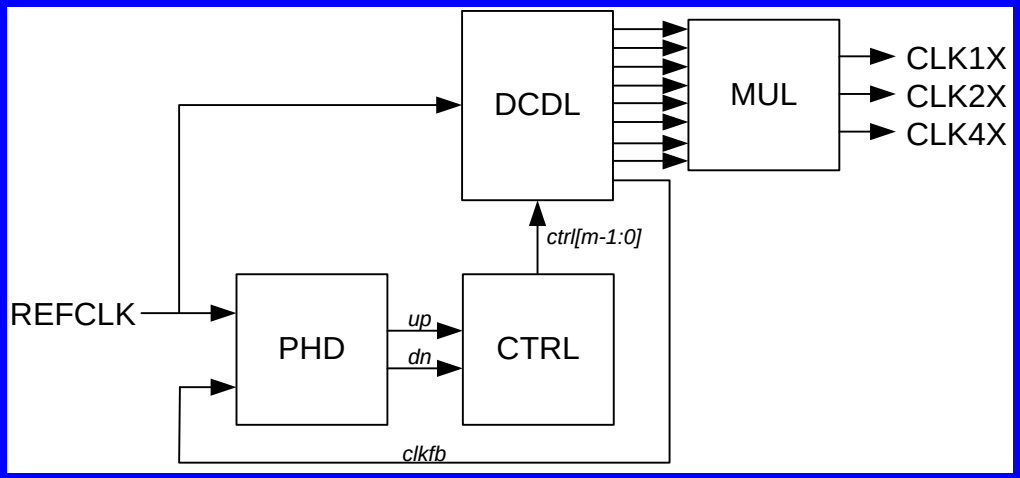


- TID affects analog transistors
- SET → unlock PLL
- SET → Phase accumulation
- False relock → Missing cycles
- Sensitive to process, voltage, temperature variations



RH all-digital DLL

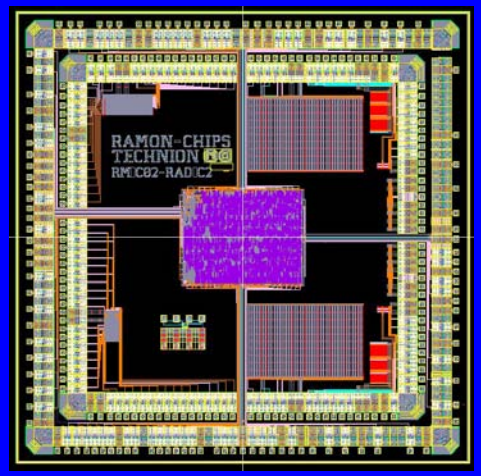
- Standard cell logic: TID, SEL protection
  - Effective over a wide range of process, voltage and temperature variations
- SEP flip-flops: SET/SEU protection
- Low jitter: typical 1% clock cycle
- Frequency multiplication by 2X,4X
- Clock de-skewing



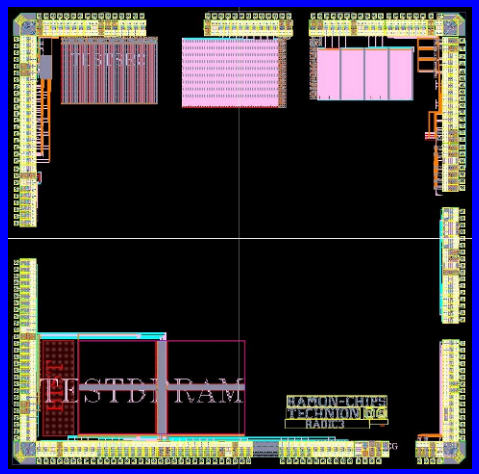
RadSafe™ libraries

- Logic
  - 80 cells, 40 Kgates/mm^2
- I/O
  - 15 cells (incl. 500 Mbps LVDS)
- SRAM
  - Single / dual port, 100 Kbit/mm^2
- DLL
- And our own methodology
  - Conversion, design, layout

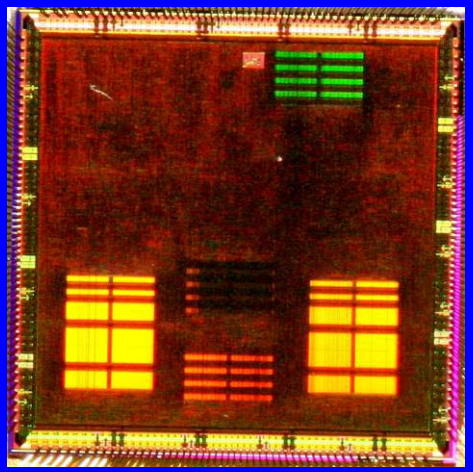
Examples of ASICs



FPGA conversion



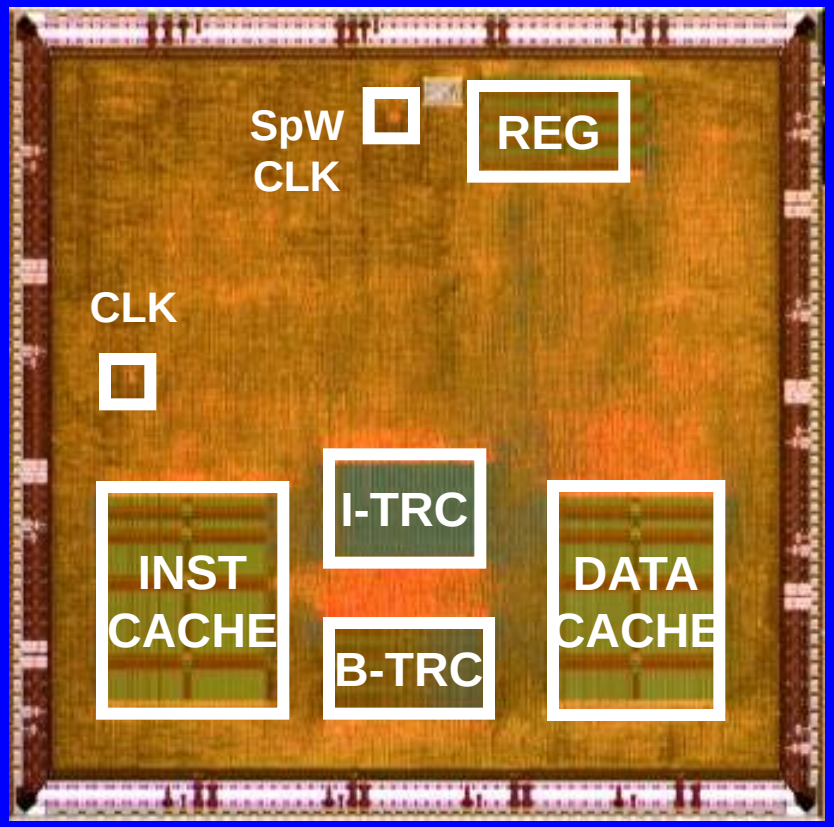
Radiation & qualification test

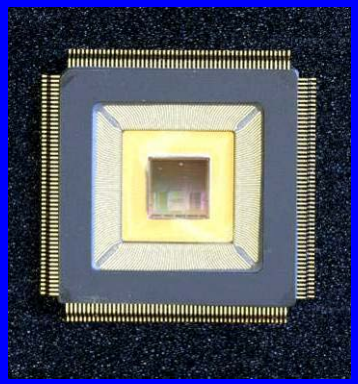


LEON3 SoC prototype

LEON3FT SoC

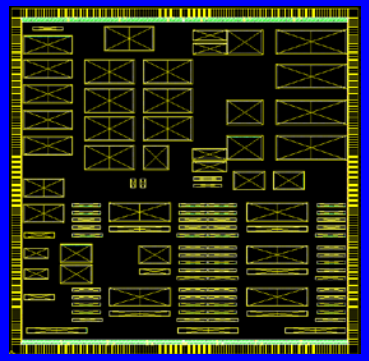
- Prototype in 2006
  - GR702RC
- Tested:
  - 120 MHz (CPU)
  - 250 Mbps (SpW)
  - All SEUs corrected





Now developing second generation...

Image Compression ASIC



- Standard JPEG2000
- 5 Mbit (250 cores), 750 Kgates
  30M transistors, 12×12mm
- Less than 3W
- Converted from Stratix-II FPGA
- For imaging satellites
  - ASIC: 44 12-bit Mpix/s, 1 Tops
  - Many ASICs in system
- Fab in 2008 ☺

Converting FPGA to ASIC

- Add mitigation
  - Enforce HDL coding rules
  - SEU detection and recovery
- Add reconfigurability
  - Never believe constants
- Verify new HDL on old FPGA+System
  - Or on FPGA-based test system

Summary

- RadSafe™
  - On commercial process, using standard EDA
  - Proven Rad-Hard-By-Design
  - High performance, low power, low cost ASICs
- Example projects
  - FPGA conversions
  - LEON3FT SoC
- Future: Now developing 0.13µ